REMARKS

Claims 12-24 and 27-33 were pending. Claims 34-35 have been added, and claims 12-13, 22, 24, and 27-28 have been amended. Accordingly, claims 12-24 and 27-35 remain pending subsequent entry of the present amendment. Support for the claim amendments and new claims can be found in at least Original claims 13 and 22, and the Description at pages 9 and 10.

In the present Office Action, claims 12-24 and 27-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,361,334 (hereinafter "Cawley"). Applicant respectfully traverses at least some of the above rejections. Nevertheless, Applicant has amended the claims to further clarify the nature of the presently claimed invention in order to facilitate a more speedy allowance of the present application. Applicant submits each of the pending claims recite features neither disclosed nor suggested by the cited art. Accordingly, reconsideration is requested.

As amended, claim 12 recites a processing system which includes

"a processor configured to

formulate an instruction and data, from a thread associated with a first context, for sending to a device, said instruction requesting the device to perform a command and return data to the processor;

store an indication in said first context which identifies a destination of said return data;

perform a context switch to switch from processing the first context to a second context prior to receiving the return data; and

a bus controller configured to generate a system bus operation to send the formulated instruction and data along with a thread identifier to the device." (emphasis added).

As seen from the highlighted features above, claim 12 recites that the processor stores an indication in the first context which identifies the destination of the return data. At least these features are absent from the cited art. In contrast to the above, Cawley merely discloses a reply may include a CPU code so that the reply can be routed to the correct CPU. For example, Cawley merely discloses:

> "The processor P is arranged to attach identifying information to each such request, in general the identifying information being returned with the reply from the memory or other unit." (Cawley, col. 4, lines 17-21).
>
> "Where multiple CPUs are fitted as indicated in FIG. 1, the identifying information in a reply received from a memory bank M, or specialised data processing unit U, includes a CPU code as well as a process code, so that the reply can be routed to the correct CPU." (Cawley, col. 5, lines 33-37).

Therefore, the above highlighted features are not disclosed by the cited art and claim 12 is patentably distinguished for at least the above reasons. As independent claim 27 includes features similar to claim 12, claims 27 is patentably distinct for similar reasons. Accordingly, all pending claims are patentably distinguished from the cited art.

Still further, the dependent claims recite features which are neither disclosed nor suggested by the cited art. For example, claim 19 recites the context register file includes for each context a write address register. In paragraph 3 of the Office Action dated July 6, 2005, it is suggested Cawley discloses these features in the following:

> "As illustrated in FIG. 2 in the case of CPU C1, each CPU, has a group of register sets R'1, R'2 . . . (referred to as contexts) for processes to be processed." (Cawley, col. 4, lines 4-7).
>
> "17. Data processing apparatus according to claim 7 programmable to operate as a data flow machine, and wherein said memory controllers comprise additional storage means for holding data transferred thereto and therefrom when the data processing system is operating as a data flow machine.

> 18. Data processing apparatus according to claim 17, in which said additional storage means include a flag field, a value field, and output list field, and an operation field to provide supply driven operation.
>
> 19. Data processing apparatus according to claim 17, in which said additional storage means includes a flag field wherein one of the flags of said flag field is a value wanted flag, a value field, an input list and an operation field to enable a demand driven operation."

Applicant submits the above cited portions of Cawley clearly do not disclose the recited context register file which includes for each context a write address register.

Still further, the features of claims 34 and 35 are wholly absent from the cited art. As recited in these claims, the processor obtains an identify of the first context (where it previously stored the destination for the return data) from the thread identifier which is returned with the data. The first context is then accessed to determine the destination for the return data and the processor writes at least a portion of the return data to the indicated destination. These features are nowhere disclosed or suggested by the cited art.

Applicant believes the application to be in condition for allowance. However, should the examiner believe issues remain, the below signed representative requests a telephone interview to facilitate a resolution.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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